

# Miniaturized Slow-Wave Coplanar Waveguide Circuits on High-Resistivity Silicon

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**Abstract** – This paper discusses slow-wave (SW) coplanar waveguide structures printed on high-resistivity silicon. Relative to a uniform line, a SW structure can reduce the guide wavelength by 45% with a 17% increase in loss per wavelength, allowing circuit miniaturization with minimal additional loss. The SW structure is demonstrated in new topologies for  $\lambda/4$  impedance transformers and an RF short. The transformer length is reduced by as much as 80% relative to a conventional design.

## I. INTRODUCTION

Slow-wave (SW) planar transmission lines have been realized in various forms since the mid-1970s. In general, a slow-wave line exhibits a phase velocity that is reduced relative to a comparable uniform line, such that the phase shift per unit length—the phase constant—is increased. The SW effect has been achieved using meandered lines, metal-insulator-semiconductor lines, and periodically loaded lines (e.g., see [1]-[5]). Recently, an interdigitated stub topology was demonstrated in the design of a low-pass filter [6].

In this paper we report on designs for loaded CPW SW structures printed on high-resistivity silicon (see Figure 1). In comparison to previous reported works, the cross-section dimensions of the CPW lines are relatively large (center conductor width of 335  $\mu\text{m}$  and slot widths of 110  $\mu\text{m}$ ) in order to minimize attenuation. Several SW designs were investigated theoretically and experimentally in order to determine the geometry with the best compromise between the slowing-factor (the ratio of the SW phase velocity to that of a uniform line) and attenuation. This basic structure was then used to develop a new, reduced-size quarter-wave impedance transformer and a SW-based RF short (90° open-circuited line).

A primary contribution of this work is to demonstrate that SW distributed transmission line circuits can be designed that have approximately the same loss as conventional implementations. A slowing-factor of 45% was achieved with only a 17% increase in the loss per

wavelength. Depending on the orientation of the SW sections, it is shown that circuit-length reductions of 50-80% are possible. These structures may be of value in reducing the circuit area of microwave/mm-wave MMIC designs.

The circuits that are discussed herein were fabricated on 400  $\mu\text{m}$ -thick, high-resistivity silicon wafers ( $\rho > 2000 \text{ Ohm-cm}$ ). The metal lines have a thickness of 1  $\mu\text{m}$ , using Cr/Ag/Cr/Au layers.

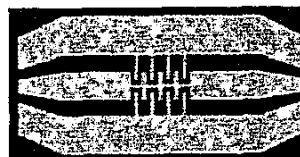


Figure 1 - Microphotograph of a four-section slow-wave CPW line on high-resistivity silicon (Type 1 – refer to Table 1).

## II. SLOW-WAVE CPW CHARACTERISTICS

A generic illustration of the CPW metal pattern for the slow-wave designs studied in this work is given in Figure 2. Using numerical electromagnetic simulation, the five designs that are detailed in Table 1 were found to exhibit an effective characteristic impedance close to 50  $\Omega$  and slowing factors ranging from 54% to 40%. Equivalent circuit models extracted from the simulation data showed the inductance and capacitance of the Type 1 SW line to be 0.98 nH/mm and 0.36 pF/mm, respectively.

As shown by the measured attenuation data in Figure 3, the attenuation per wavelength in the SW designs increases as the phase velocity is reduced. In each case, the “wavelength” corresponds to a 360° electrical length for the particular geometry. (The data for a slow-wave factor of 1 corresponds to measured insertion loss for a uniform CPW delay line that was used during the

calibration sequence.) The attenuation for the Type 1 SW structure, which exhibits the 54% slow-wave factor, is only 17% higher than the uniform line. As Types 2-4 have increasing perturbations in the center and ground conductors, the steady increase in loss as the phase velocity is reduced can be attributed to longer current paths.

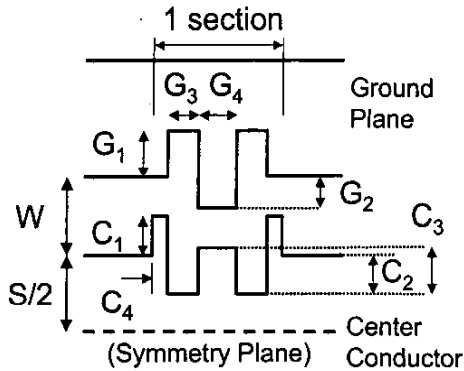


Figure 2 - Geometrical parameters for the slow-wave CPW structures (upper half of line only).

Table 1 - Characteristics of different slow-wave CPW lines (all dimensions in microns). For all designs, the center conductor width (S) is 335 microns and the slot width (W) is 110 microns (see Figure 2).

SW-Type	1	1B	2	3	4
C1	0	0	0	80	80
C2	97	97	97	97	97
C3	0	0	0	0	0
C4	50	50	50	50	50
G1	0	0	97	97	200
G2	177	177	177	177	177
G3	25	75	25	25	25
G4	30	30	30	30	30
Slowing Factor	54%	----	50%	44%	40%

Measurement data for multiple-section Type 1 SW structures demonstrate that the characteristics are maintained as the overall line length increases. The effective relative dielectric constant, extracted from 2-through 16-section SW structures was 20.5 +/- 1.5 through 40 GHz (Figure 4). The return loss for the same lines, relative to 50  $\Omega$ , was greater than 25 dB until 37 GHz (Figure 5).

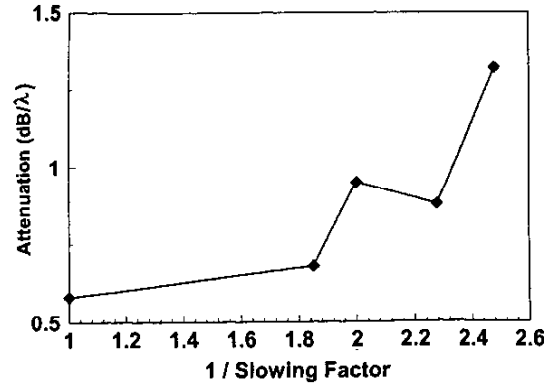


Figure 3 - Measured attenuation per guide wavelength versus inverse slow-wave factor at 20 GHz.

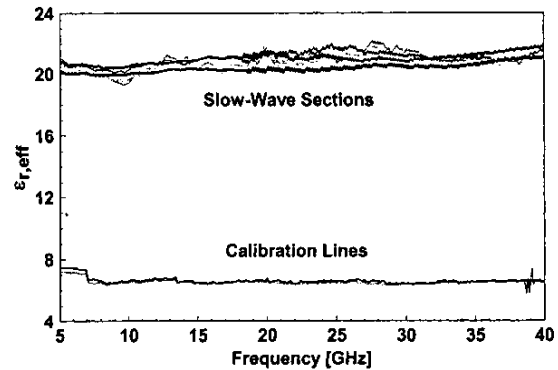


Figure 4 - Effective relative dielectric constant for Type 1 SW structures (2-, 3-, 4-, 8-, and 16-sections). Results for a uniform CPW calibration line are shown for comparison.

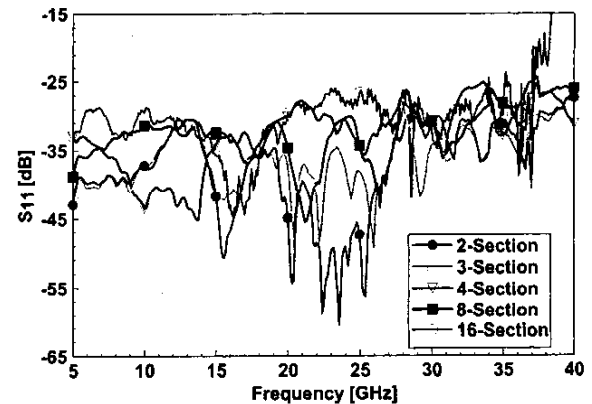


Figure 5 - Measured  $S_{11}$  for Type 1 SW structures (2-, 3-, 4-, 8-, and 16-sections).

### III. SW $\lambda/4$ IMPEDANCE TRANSFORMERS

A photograph of a new type of SW-based quarter-wavelength impedance transformer is shown in Figure 6. Here the SW geometry is perpendicular to the longitudinal axis of the uniform CPW feedlines. As there are no air-bridges or bond-wires to equalize the ground planes, the circuit does not operate as would a parallel stub-loaded transmission line. Rather, there is a forward propagating, mixed CPW-slotline mode behavior.

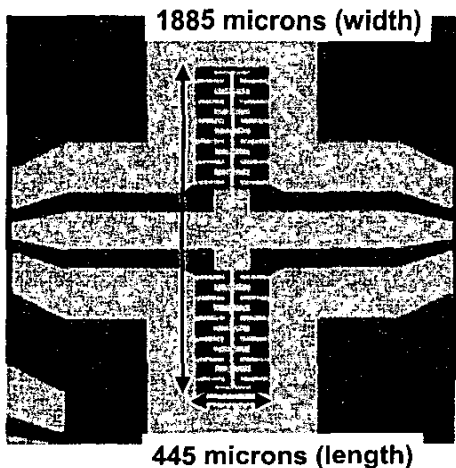


Figure 6 – Microphotograph of a 6-section Type 1 SW impedance transformer. The  $\lambda/4$  frequency is 11 GHz and the transformer impedance is 19  $\Omega$ .

Representative characteristics of a 4-section, 14 GHz Type 1 SW impedance transformer are shown in Figure 7. The length and width are 445 and 1450  $\mu\text{m}$ , respectively (refer to the 6-section design in Figure 6); applying the 54% slow-wave factor for Type 1 designs, the mean path length around the top/bottom slot is  $\sim 90^\circ$  at 14 GHz. The characteristics of the SW transformer tend to resemble an ideal transmission line response around the quarter-wave frequency  $\pm 20\%$ . The effective characteristic impedance of the transformer is 21  $\Omega$ , resulting in an impedance transformation between 50  $\Omega$  and 9  $\Omega$ , as shown by the input impedance plot in Figure 7. At 14 GHz, the SW design provides a *length* reduction of 80% relative to a straight  $\lambda/4$ -section of uniform CPW line. While a uniform line could in practice be bent vertically as is the SW geometry, the width of the uniform structure

would be  $\sim 2\times$  that of the SW design.

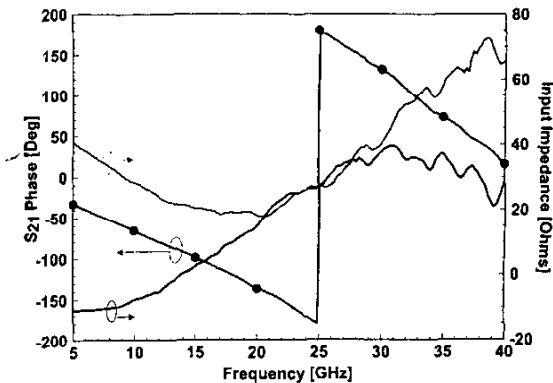


Figure 7 –  $S_{21}$  phase and input impedance for a 4-section Type 1 SW impedance transformer terminated in 50  $\Omega$ .

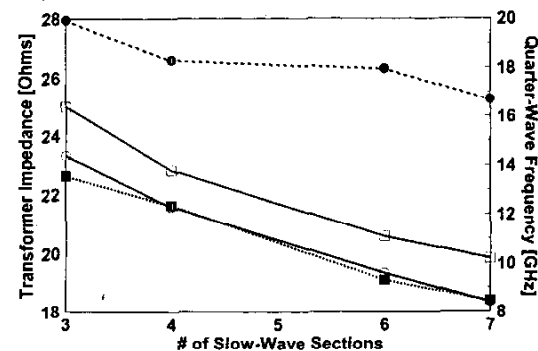


Figure 8 – Measured characteristics of SW impedance transformers. (Solid markers - transformer impedance; open markers - quarter-wave frequency. Circles – Type 1 SW; squares – Type 1B SW.)

The basis for the assertion of mixed CPW-slotline behavior derives from the observed characteristics of different-sized transformer designs. The effective transformer impedance and center frequency for 3-, 4-, 6- and 7-section configurations, using Type 1 and Type 1B SW designs, are shown in Figure 8. As would be expected, the center frequency decreases as the number of sections---and therefore the mean path length through the transformer---increases. There is also, however, a steady decrease in the transformer impedance as the number of sections increases. This can be explained by considering the longitudinal slot lengths at the top and bottom extremes of the geometry operating as a CPW section with a wide center conductor. The lower impedance values for

Type 1B designs is consistent in this regard, as the vertical displacement is larger than that of the Type 1 designs by  $N \times 100$  microns, where  $N$  is the number of sections (refer to the G3 dimension Table 1).

#### IV. SW RF SHORT

In MMIC design, RF shorts are used to realize a zero impedance point at a specific frequency without using a DC path to ground. Two common methods of achieving an RF short are to use a quarter-wavelength open-circuited line or a large shunt capacitor. Quarter-wave lines occupy considerable wafer real estate, however, and capacitors may require the need for otherwise unnecessary fabrication steps.

The slow-wave structures can be used to significantly reduce the length of the RF short. A direct approach would be to use an open-circuited line such as that shown in Figure 1; using the slowing-factor of 54% for a Type 1 structure the required offset to the short-circuit position would be  $\sim 2\times$  less than that for a uniform line. An alternative approach is to use an asymmetric SW geometry such as the one shown in Figure 9. In this case the phase delay through the uniform slot lags the delay through the SW slot, resulting in a capacitive termination at the bottom of the structure.

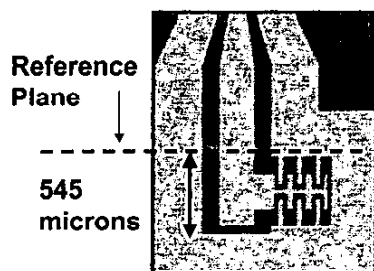


Figure 9 – Microphotograph of a 3-section Type 1 slow-wave CPW RF short.

For a design comprised of 7 slow-wave sections in the lateral slot region, an RF short occurs at the reference plane indicated in Figure 9 at 14 GHz (see Figure 10). At this frequency, the 545 micron distance from the end of the stub is  $\sim 23^\circ$ , which equates to a 75% reduction compared to a uniform  $90^\circ$  open-circuit line. The return loss at 14 GHz is approximately 0.5 dB.

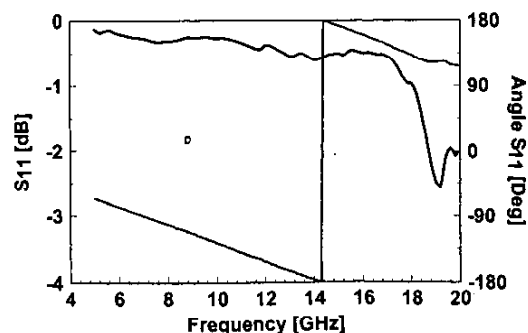


Figure 10 – Measured  $S_{11}$  for a 7-section SW circuit of the type shown in Figure 9.

#### V. SUMMARY

The use of periodically loaded slow-wave transmission lines is an effective approach to achieving reduction ratios of 50% and higher for distributed transmission line circuits. The Type 1 geometry presented herein exhibits a slowing factor of 54% with a marginal (17%) increase in the loss per wavelength. With this line, circuit designs based on electrical delay can be miniaturized without a significant increase in attenuation. While this work used silicon as the substrate material, similar results would be obtained for other high dielectric constant materials such as alumina and GaAs.

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